What is claimed is:

1. A transistor device comprising:

a semiconductor region having a top surface;

a source region in the semiconductor region;

a drain region in the semiconductor region;

a channel region in the semiconductor region between the source region and the drain region;

an impurity region within the channel region and spaced from the top surface, the impurity region laterally spaced from the source and drain regions;

a gate overlying the channel region; and

a gate dielectric between the gate and the channel region.

2. The device of claim 1 wherein the semiconductor region comprises a region of monocrystalline silicon.

3. The device of claim 2 wherein the semiconductor region comprises a silicon substrate.

4. The device of claim 1 wherein the source and drain regions extend into the semiconductor region a first distance, and wherein the impurity region is spaced from the top surface by a distance less than the first distance.

5. The device of claim 1 wherein the gate dielectric comprises silicon dioxide.

6. The device of claim 1 wherein the impurity region comprises a region of an implanted oxygen bearing species in the channel region.

7. The device of claim 1 wherein the channel region comprises a strained channel region.

8. The device of claim 1 and further comprising:

a first sidewall spacer adjacent a first sidewall of the gate;

a second sidewall spacer adjacent a second sidewall of the gate;

a lightly doped drain region within the semiconductor region adjacent the drain region, the lightly doped drain region disposed beneath the first sidewall; and

a lightly doped source region within the semiconductor region adjacent the source region, the lightly doped source region disposed beneath the second sidewall.

9. The device of claim 1 and further comprising a second transistor, the second transistor including:

a second source region in the semiconductor region;

a second drain region in the semiconductor region;

a second channel region in the semiconductor region between the second source region and the second drain region;

a second gate overlying the channel region; and

a second gate dielectric between the gate and the channel region.

10. The device of claim 9 further comprising a second impurity region within the second channel region and spaced from the top surface, the second impurity region laterally spaced from the second source region and the second drain region.

11. The device of claim 9 wherein the second transistor does not include an impurity region within the second channel region.

12. The device of claim 9 wherein the second transistor device comprises an n-channel transistor.

13. A method of forming a transistor device, the method comprising:

providing a semiconductor region having a top surface;

forming source and drain regions in the semiconductor region, the source region being spaced from the drain region by a channel region;

forming an oxide region within the channel region and spaced from the top surface; and

forming a gate overlying and insulated from the channel region.

14. The method of claim 13 wherein the oxide region is formed before forming the source and drain regions.

15. The method of claim 13 wherein the oxide region is formed after forming the source and drain regions.

16. The method of claim 13 wherein forming an oxide region comprises implanting an oxygen bearing species.

17. The method of claim 16 wherein the oxygen bearing species comprises O_2.

18. The method of claim 16 wherein forming an oxide region further comprises annealing the transistor device after implanting the oxygen bearing species.

19. The method of claim 13 wherein the step of forming source and drain regions includes forming lightly doped source and drain regions.

20. The method of claim 13 wherein the step of forming source and drain regions includes forming heavily doped source and drain regions.

21. The method of claim 13 wherein forming the gate includes forming a gate dielectric between the gate and the channel region.

22. The method of claim 13 wherein the gate dielectric comprises silicon dioxide.

23. The method of claim 21 wherein forming the gate includes forming a poly-silicon layer on top of the gate dielectric.

24. The method of claim 13 wherein the semiconductor region comprises a silicon substrate.

25. The method of claim 13 further comprising:

forming a first sidewall spacer adjacent a first sidewall of the gate;

forming a second sidewall spacer adjacent a second sidewall of the gate;

forming a lightly doped drain region within the semiconductor region adjacent the drain region, the lightly doped drain region disposed beneath the first sidewall; and

forming a lightly doped source region within the semiconductor region adjacent the source region, the lightly doped source region disposed beneath the second sidewall.

26. A method of manufacturing a CMOS device, the CMOS device including a P-channel MOSFET and an N-channel MOSFET, the method comprising:

providing a semiconductor region having a top surface;

forming source and drain regions for the P-channel MOSFET in a first part of the semiconductor region, the source region being spaced from the drain region by a P-channel region;

forming source and drain regions for the N-channel MOSFET in a second part of the semiconductor region, the source region being spaced from the drain region by an N-channel region;

forming at least one oxide region in the semiconductor region spaced from the top surface; and

forming a gate for the P-channel MOSFET and a gate for the N-channel MOSFET, the gate for the P-channel MOSFET overlying and insulated from the P-channel region, and the gate for the N-channel MOSFET overlying and insulated from the N-channel region.

27. The method of claim 26 wherein forming at least one oxide region includes forming an oxide region between the source and drain regions for the P-channel MOSFET.

28. The method of claim 26 wherein forming at least one oxide region includes forming an oxide region between the source and drain regions for the N-channel MOSFET.

29. The method of claim 26 wherein forming at least one oxide region includes:

forming a first oxide region between the source and drain regions for the P-channel MOSFET; and

forming a second oxide region between the source and drain regions for the N-channel MOSFET.